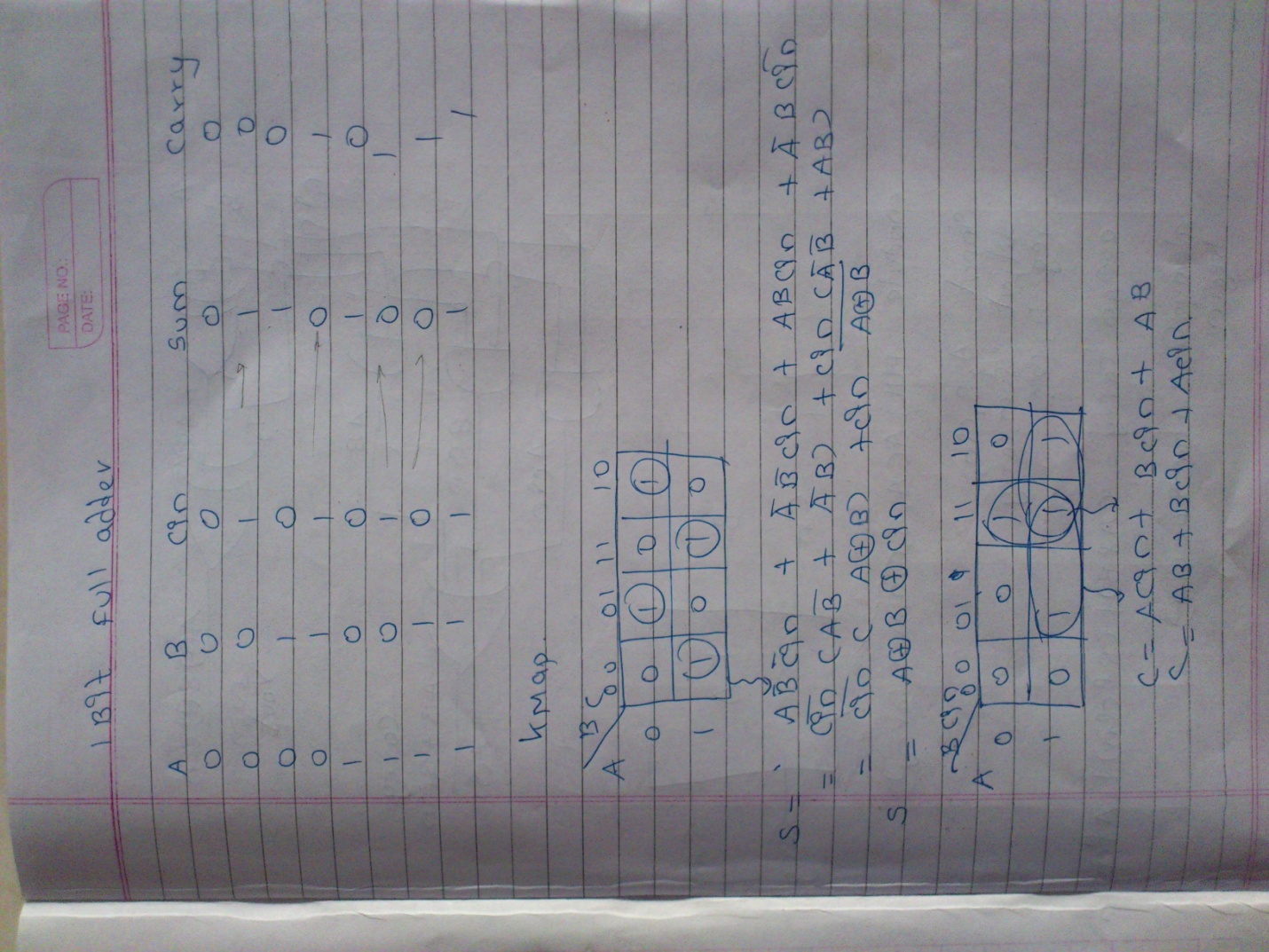
**Homework assignment Q.no 4)**

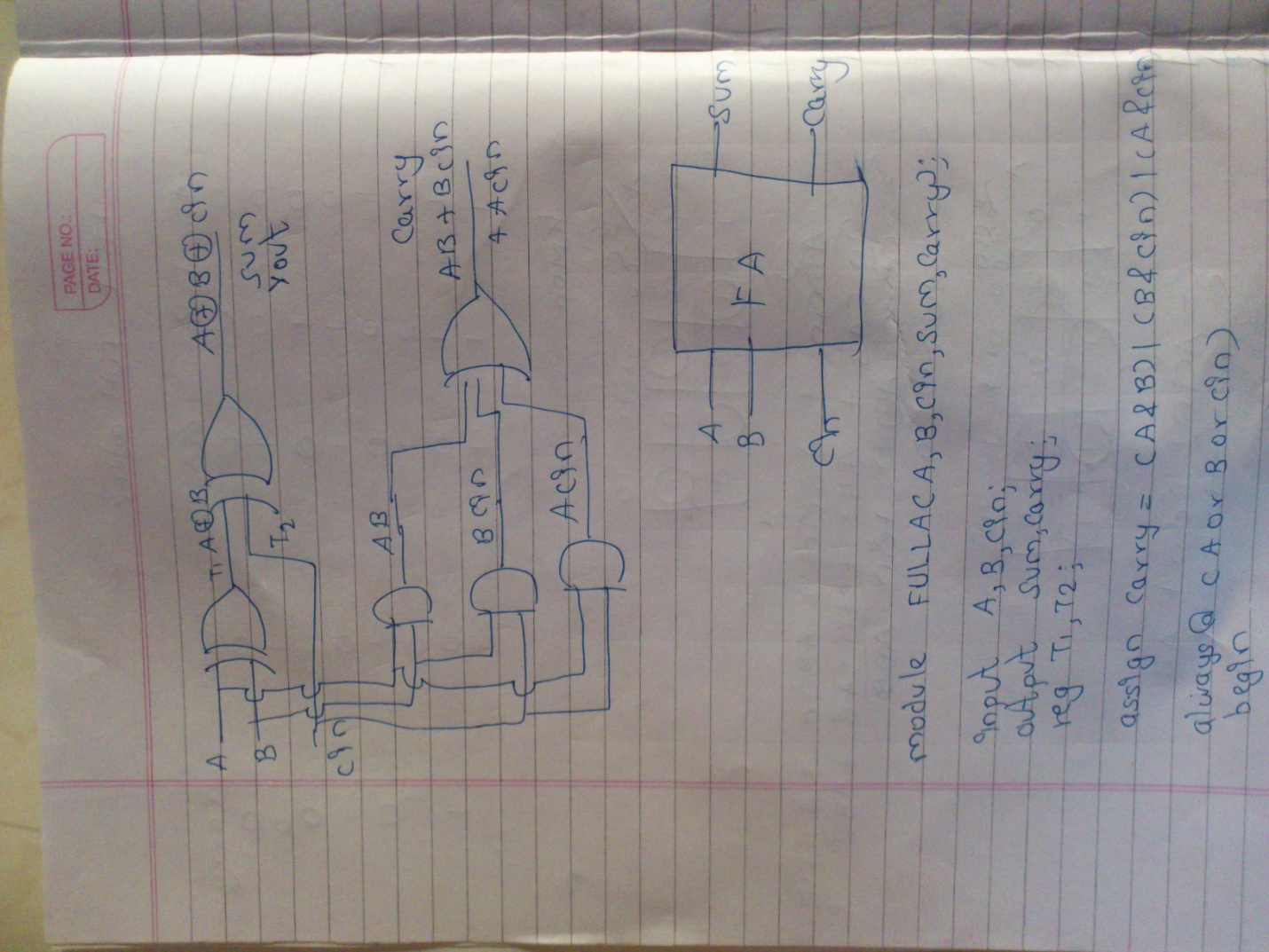
**1)Understanding the Problem:**

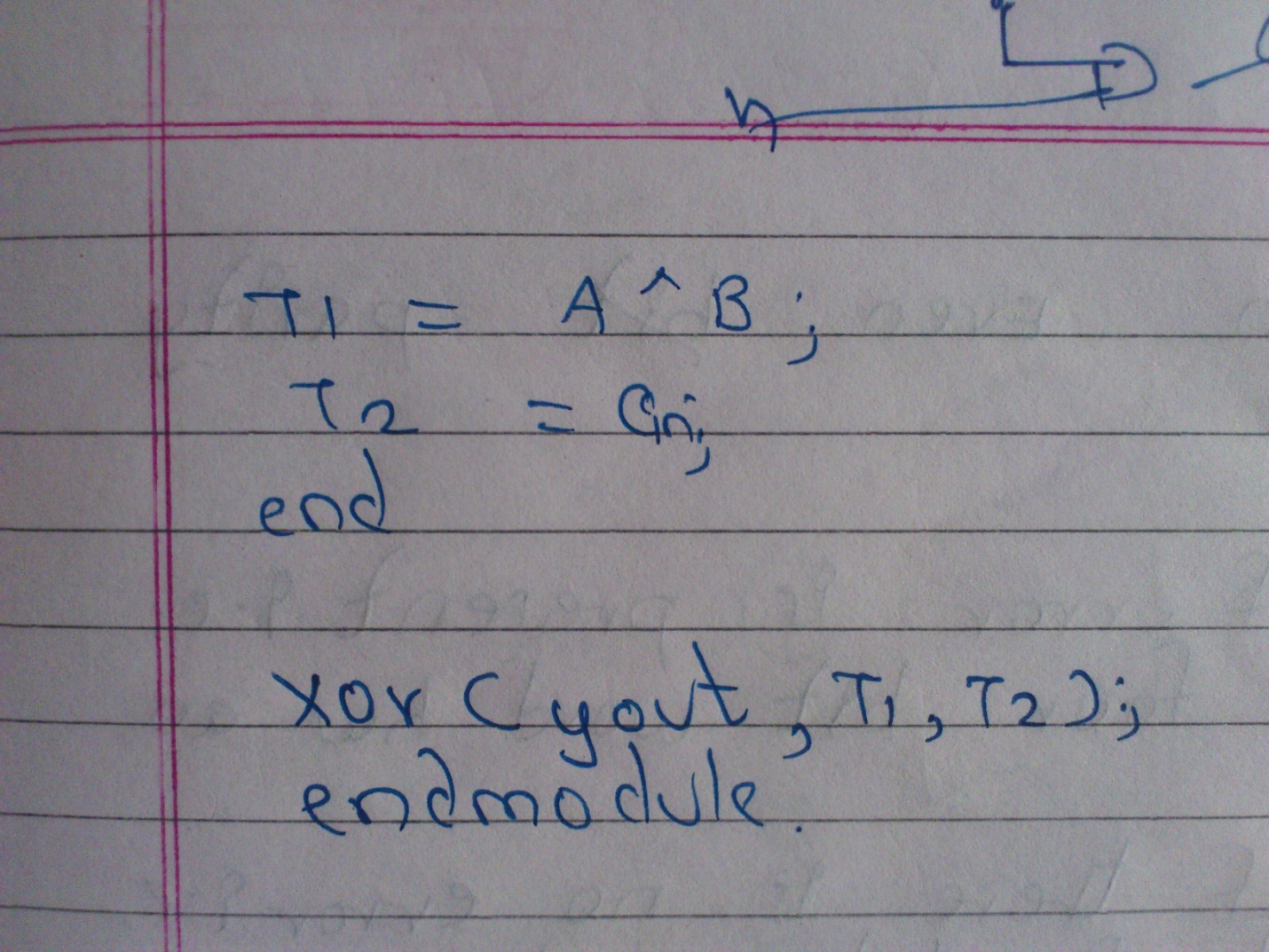
In this program we have to design a 1 bit full adder & also implement a 4 bit Ripple carry Adder using the 1 bit full adder.It is asked to use a mix style of modeling in the above question. So we have to use all types of modeling. We have to use module instantiation in above program.

**2) Devising a Plan/Design:**

We need to get the expression for Sum and Carry from the Truth Table.Then data flow modeling is used for Carry & Behavioural & Structural Modelling is used for Sum.Proper Syntax for types need to be followed.Also module Instantiation is used for 4 bit Ripple carry Adder.







1. **Carrying out the plan:**

**Verilog code:**

module fulladder(

input wire a,

input wire b,

input wire cin,

output Sum,

output Carry

);

reg T1,T2;

assign Carry=(a&b)|(b&cin)|(a&cin);//Data flow modelling

always@(a or b or cin) //Behavioural Modelling

begin

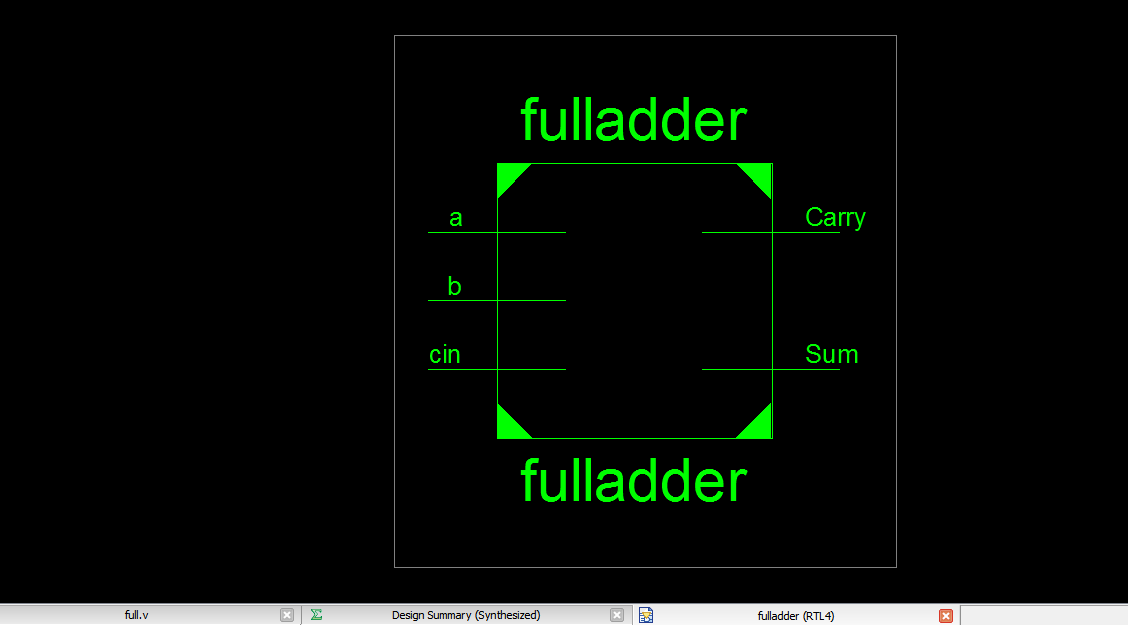
T1=a^b;

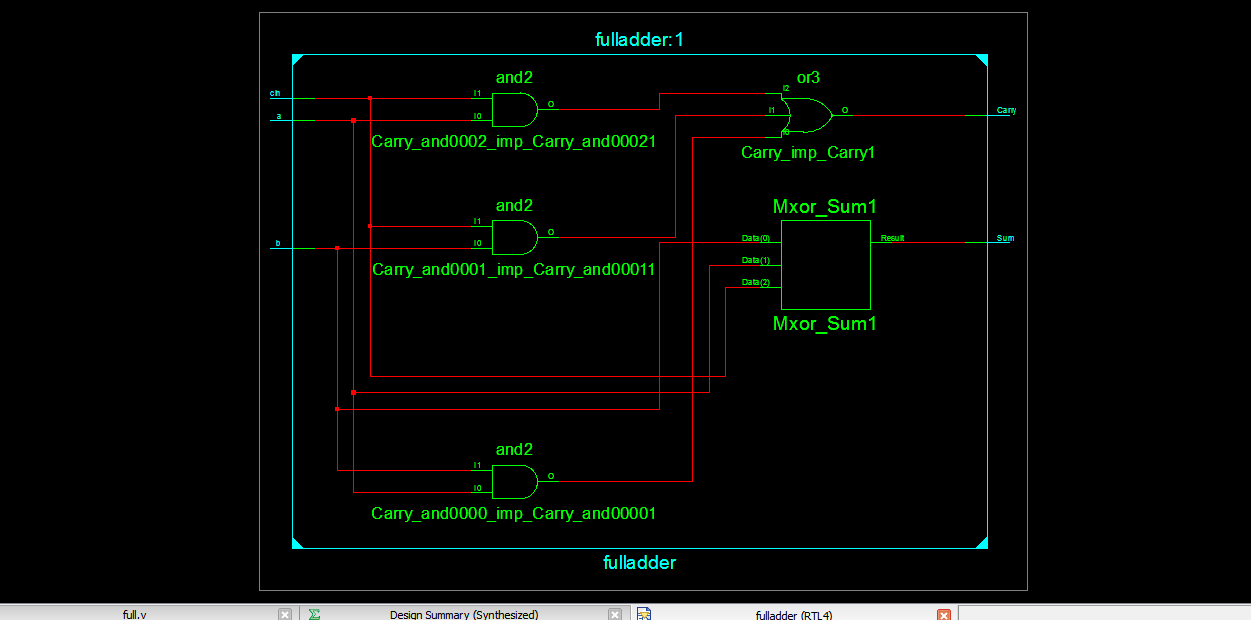
T2=cin;

end

xor(Sum,T1,T2);// Structural modelling

endmodule





**Test Bench:**

module fulladder\_tb;

// Inputs

reg a;

reg b;

reg cin;

// Outputs

wire Sum;

wire Carry;

// Instantiate the Unit Under Test (UUT)

fulladder uut (

.a(a),

.b(b),

.cin(cin),

.Sum(Sum),

.Carry(Carry)

);

initial begin

// Initialize Inputs

a = 0;

b = 0;

cin = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

a=1'b1;

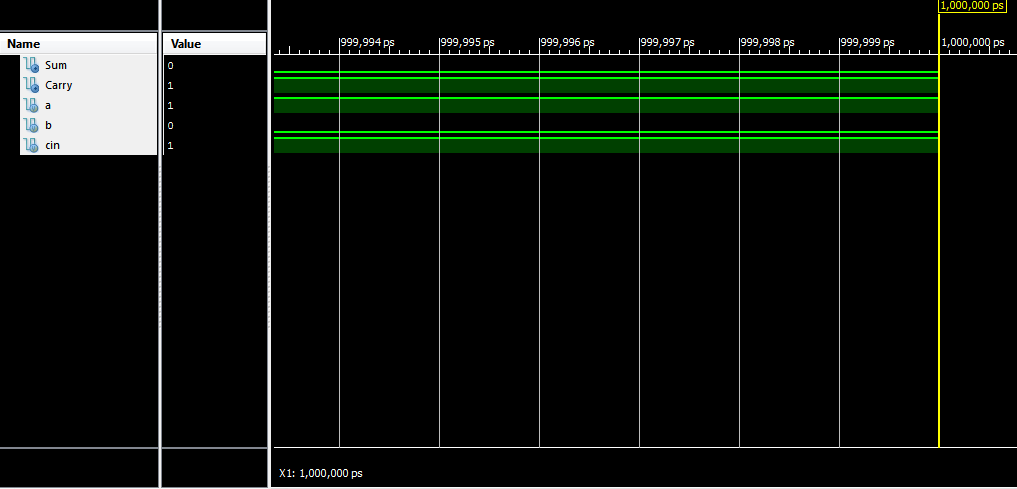
b=1'b0;

cin=1'b1;

#100;

end

endmodule



**4 bit Ripple Carry Adder**

module fourbit(input a3,input a2,input a1,input a0,input b3,input b2,input b1,input b0,input cin0,

output s3,output s2,output s1,output s0,output Carry4);

wire Carry1,Carry2,Carry3;

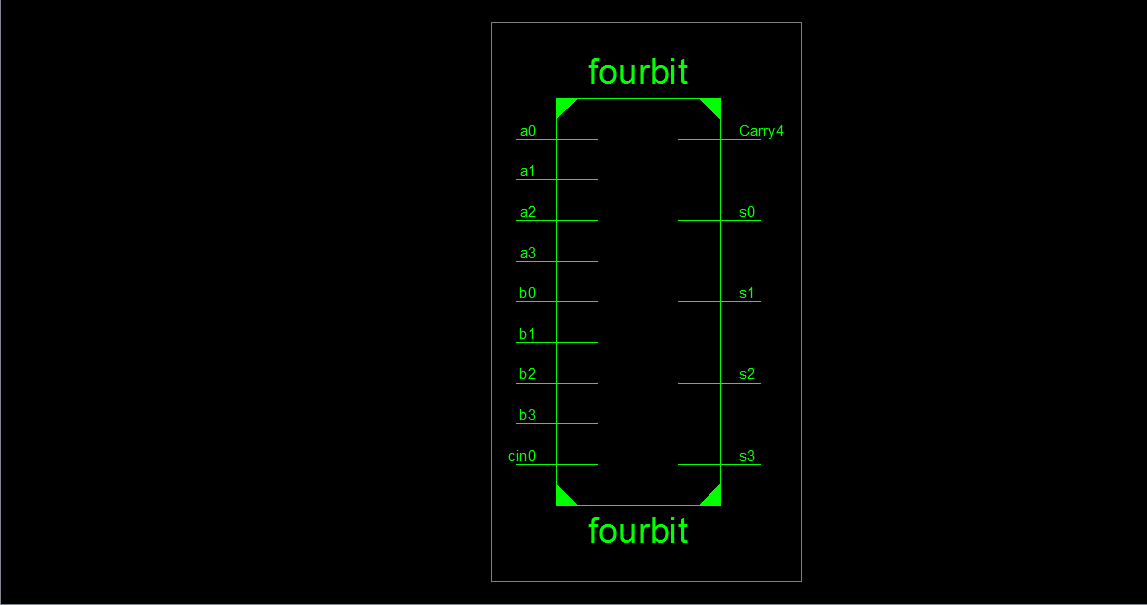
fulladder fa\_0( a0, b0, cin0, s0, Carry1);

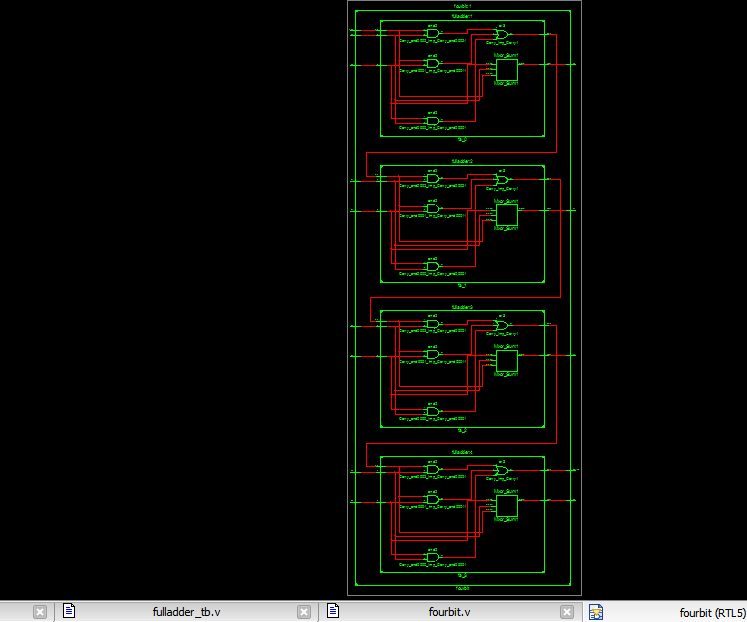
fulladder fa\_1( a1, b1, Carry1, s1, Carry2);

fulladder fa\_2( a2, b2, Carry2, s2, Carry3);

fulladder fa\_3( a3, b3, Carry3, s3, Carry4);

endmodule





1. **Looking back i.e. Self reflection:**

In the above program we designed a 1 bit full adder & instantiated its module to design a 4 bit ripple carry adder. We learnt the technique of module instantiation & Hierarchical programming.

***Synthesis report:***

Release 12.1 - xst M.53d (nt)

Copyright (c) 1995-2010 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.39 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.41 secs

--> Reading design: fourbit.prj

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6.1) Advanced HDL Synthesis Report

7) Low Level Synthesis

8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

=========================================================================

\* Synthesis Options Summary \*

=========================================================================

---- Source Parameters

Input File Name : "fourbit.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "fourbit"

Output Format : NGC

Target Device : xc3s200-5-pq208

---- Source Options

Top Module Name : fourbit

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : lut

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : YES

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : YES

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Library Search Order : fourbit.lso

Keep Hierarchy : NO

Netlist Hierarchy : as\_optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=========================================================================

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling verilog file "fulladder.v" in library work

Compiling verilog file "fourbit.v" in library work

Module <fulladder> compiled

Module <fourbit> compiled

No errors in compilation

Analysis of file <"fourbit.prj"> succeeded.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for module <fourbit> in library <work>.

Analyzing hierarchy for module <fulladder> in library <work>.

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing top module <fourbit>.

Module <fourbit> is correct for synthesis.

Analyzing module <fulladder> in library <work>.

Module <fulladder> is correct for synthesis.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <fulladder>.

Related source file is "fulladder.v".

Found 1-bit xor3 for signal <Sum>.

Summary:

inferred 1 Xor(s).

Unit <fulladder> synthesized.

Synthesizing Unit <fourbit>.

Related source file is "fourbit.v".

Unit <fourbit> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Xors : 4

1-bit xor3 : 4

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Xors : 4

1-bit xor3 : 4

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

Optimizing unit <fourbit> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block fourbit, actual ratio is 0.

Final Macro Processing ...

=========================================================================

Final Register Report

Found no macro

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

=========================================================================

\* Final Report \*

=========================================================================

Final Results

RTL Top Level Output File Name : fourbit.ngr

Top Level Output File Name : fourbit

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs : 14

Cell Usage :

# BELS : 8

# LUT3 : 8

# IO Buffers : 14

# IBUF : 9

# OBUF : 5

=========================================================================

Device utilization summary:

---------------------------

Selected Device : 3s200pq208-5

Number of Slices: 4 out of 1920 0%

Number of 4 input LUTs: 8 out of 3840 0%

Number of IOs: 14

Number of bonded IOBs: 14 out of 141 9%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

No clock signals found in this design

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 12.008ns

Timing Detail:

--------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default path analysis

Total number of paths / destination ports: 33 / 5

-------------------------------------------------------------------------

Delay: 12.008ns (Levels of Logic = 6)

Source: b0 (PAD)

Destination: Carry4 (PAD)

Data Path: b0 to Carry4

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 2 0.715 1.040 b0\_IBUF (b0\_IBUF)

LUT3:I0->O 2 0.479 0.915 fa\_0/Carry1 (Carry1)

LUT3:I1->O 2 0.479 0.915 fa\_1/Carry1 (Carry2)

LUT3:I1->O 2 0.479 0.915 fa\_2/Carry1 (Carry3)

LUT3:I1->O 1 0.479 0.681 fa\_3/Carry1 (Carry4\_OBUF)

OBUF:I->O 4.909 Carry4\_OBUF (Carry4)

----------------------------------------

Total 12.008ns (7.540ns logic, 4.468ns route)

(62.8% logic, 37.2% route)

=========================================================================

Total REAL time to Xst completion: 6.00 secs

Total CPU time to Xst completion: 5.72 secs

-->

Total memory usage is 186424 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)